EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	5	(("5678016") or ("5732005") or ("5764959") or ("6138135") or ("6282634")).PN.	US-PGPUB; USPAT	OR	OFF	2007/01/03 11:36
S2	5	("5341320" | "5481489" | "5631859" | "5732005" | "6049865").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/01/03 11:38
S3	12	("6138135").URPN.	USPAT	OR	ON	2007/01/03 11:39
S4	15	("4135249" | "4403284" | "4476537" | "4620292" | "4748580" | "4785412" | "4805128" | "4901233" | "5019961" | "5027272" | "5140687" | "5197005" | "5274679" | "5317526" | "5341506").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/01/03 11:39
S5	5	("5732005").URPN.	USPAT	OR	ON	2007/01/03 11:40
S6	157	703/26.ccor.	US-PGPUB; USPAT	OR	ON	2007/01/03 11:40
S7	101	708/495.ccor.	US-PGPUB; USPAT	OR	ON	2007/01/03 11:40
S8	26957	floating adj point	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/03 12:51
S9	10091	S8 with (hardware unit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/03 12:58
S10	2837	S9 and precision	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/03 12:58
S11	635	S10 and emulat$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/03 12:59
S12	191	S11 and exponent	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/03 12:59
S13	73	S12 and mantissa	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/03 13:00
S14	65	S13 and integer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/03 13:00
S15	61	S14 and @ad<="20031202"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/03 13:01
S16	4	("3930232" | "4041292" | "4722068" | "5341321").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/01/03 13:03
S17	22	("5631859").URPN.	USPAT	OR	ON	2007/01/03 13:04

		Results
5.	(((pub-date > 1959 and pub-date < 2004 and FULL-TEXT(floating point) and FULL-TEXT(precision)) and emulat!) and integer) and mantissa *[All Sources(- All Sciences -)]*	12
4.	(((pub-date > 1959 and pub-date < 2004 and FULL-TEXT(floating point) and FULL-TEXT(precision)) and emulat!) and integer) and exponent *[All Sources(- All Sciences -)]*	18
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#3	(((floating point unit)<or>(floating point hardware) <and>precision)<and>exponent<and>mantissa<and>integer) <and> (pyr >= 1951 <and> pyr <= 2003)	50
#4	(((floating point unit)<or>(floating point hardware) <and>precision) <and>exponent<and>mantissa<and>integer<and>emulat*) <and> (pyr >= 1951 <and> pyr <= 2003)	11

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The Internet Streaming SIMD Extensions - Thakkar, Huff (1999) (Correct) (17 citations)
arcade consoles to workstation applications. **Floating-point** (FP) computation is the heart of 3D geometry III processor was problematic because of its **emulation** of 4-wide SIMD-FP. Using packed instructions of the new extension was accelerating single **precision floating-point** computation, which involved the developer.intel.com/technology/itj/q21999/articles/../pdf/simd_ext.pdf

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Realization of PRAMs: Processor Design - Jörg Keller, Wolfgang J. Paul.. (1994) (Correct) (15 citations)
for a prototype VLSI implementation with a **floating point** unit. 1 Introduction Parallel programming set and provides in hardware mechanisms for the **emulation** of shared memory: random hashing to avoid hot need only one opcode format and that only single-**precision floating-point** instructions are supported. We www-wjp.cs.uni-sb.de/projects/sbpram/papers/wdag94final.ps.gz

A pragmatic approach to compilation of Erlang - Johansson, Jonsson, Lindgren (1997) (Correct) (3 citations)
be either fixed **precision integers** (fixnums)**floating point** numbers, or arbitrary **precision integers** which use different execution models: bytecode **emulation** (JAM)and compilation to machine code via C expression in Erlang can be either fixed **precision integers** (fixnums)**floating point** numbers, or vodka.lfcia.org/erlang/pacomp_Erlang.ps

Numerical Computation Guide - Microsystems (1996) (Correct) (2 citations)
.1 **Floating-Point** Environment .
192.18.99.138/802-5692/802-5692.pdf

Detecting and Exploiting Narrow Bitwidth Computations - Budiu, Goldstein (1999) (Correct) (2 citations)
module library can be used to build fixed- or **floating-point** operations from these primitives. A DIL value the bigger the emulated circuit, the longer the **emulation** of a clock cycle takes. Reducing the number and All data values manipulated by DIL are arbitrary **precision integer** values. A module library can be used to www.cs.cmu.edu/~mihaib/research/socs2.ps.gz

Injection Of Faults In Complex Computers - Henrique Madeira Joo (1995) (Correct) (1 citation)
user defined events such as load, store, or **floating point** instructions, while the latter enable the fault injection techniques, also known as fault **emulation** (e.g.Segall 88, Chillarege 89, Han 93, Young degrees) these kind of features are the HP **Precision** architecture, the PowerPC family, the Pentium, dsg.dei.uc.pt/Papers/wetds95.ps.Z

Automatic Evaluation of the Accuracy of Fixed-point Algorithms - Menard, Sentieys (2002) (Correct)
for the automatic implementation of **floating-point** algorithms in fixed-point architectures. In with the increase of execution time due to the **emulation** of the fixed-point mechanisms, leads to long word-length of the data as long as the desired **precision** constraints are respected. The most common used www.sigda.org/Archives/ProceedingArchives/Date/Date2002/papers/2002/date02/htmfiles/sun_sgi/../../pdffiles/05e_4.pdf

Mapping of Speech Front-End Signal Processing to High Performance .. - Moretto (1995) (Correct)
Standard Mips Risc Microprocessor With No-**Floating Point** Unit And An Additional Fixed Point Vector and IEEE single **precision floating-point emulation**. The majority of the routines are written in through linear interpolation, and IEEE single **precision floating-point emulation**. The majority of the www.ICSI.Berkeley.EDU/ftp/global/pub/techreports/1995/tr-95-063.ps.gz

32-bit Logarithmic ALU for Handel C 2.1 and.. - Kadlec, Hermanek, .. (Correct)
UK. Abstract Implementation of IEEE **floating point** in FPGA (Field Programmable Gate Array) is } Corresponding CODE in Matlab, using HSLA **emulation** library: for k=1:8, la2(lsq2(lm2(are arithmetic (ADD, SUB, MUL, DIV and SQRT)with **precision** equal to or better than: the standard IEEE www.celoxica.com/products/technical_papers/../../products/technical_papers/academic_papers/Lns2CelRev2.pdf

Numerical Error Minimizing Floating-Point to Fixed-Point ANSI.. - Aamodt, Chow (1999) (Correct)
Numerical Error Minimizing **Floating-Point** to Fixed-Point ANSI C Compilation Tor Aamodt

large processor die areas, or slow software **emulation**. In many embedded applications the resulting
to 1.1, 0.5, 1.0, and 2.1 extra bits of **precision** carried throughout the computations are shown
www.eecg.utoronto.ca/~aamodt/papers/MPDSP-minerr.pdf

Floating Point to Fixed Point Conversion of C Code - Cilio, Corporaal (1999) (Correct)
Floating Point to Fixed Point Conversion of C Code Andrea G.
fixed-point arithmetic instead of **floating-point emulation** trades off computation accuracy for execution
To avoid overflows and reduce the loss of **precision** he must scale the **integer** words. Determining
cardit.et.tudelft.nl/MOVE/papers/Cilio99a.ps.gz

Fixed-point arithmetic for ASIP code generation - Cilio, Karkowski, Corporaal (1998) (Correct)
impact on the accuracy when compared to a **floating-point** version of the same program. In the same time
times faster than its equivalent **floating-point emulation** on an **integer** datapath. 1 Introduction In
To avoid overflows and reduce the loss of **precision** he must scale the **integer** words. Determining
cardit.et.tudelft.nl/MOVE/papers/cilio98a.ps

Why 64 Bit Computers in the Control - Room By (Correct)
prices, 16 GB would cost $640K. 64 Bit Data **Floating point** data types have been 64 bits or more for many
32 bit systems typically provide software **emulation** for formats with greater than 32 bits,
format provides 64 bit and 128 bit formats for **precision** and accuracy. 32 bit systems typically provide
www.digital.com/info/LI01PK/LI01PKP8.PS

A Software-Oriented Floating-Point Format for Enhancing.. - Yamada, Connors, Hwu (1998) (Correct)
A Software-Oriented **Floating-Point** Format for Enhancing Automotive Control
for automotive control programs that use software **emulation** rather than hardware resources. Since the
the compiler to customize the format's range and **precision** for automotive control systems. At the same
ftp.crhc.uiuc.edu/pub/IMPACT/conference/case-98-float.ps

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SH4 RISC multimedia microprocessor - group of 5 »
F Arakawa, O Nishii, K Uchiyama, N Nakagawa - Micro, IEEE, 1998 - ieeexplore.ieee.org
... performance of, for example, **integer** processing ... is wider than the single- **precision mantissa** width, and ... Floating-point transform vector **instruction** FTRV uses a ...
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SH4 RISC Microprocessor for Multimedia - group of 3 »
F Arakawa, O Nishii, K Uchiyama, N Nakagawa - HOT Chips IX Symposium Record, Aug, 1997 - mobile.ss.titech.ac.jp
... ID: **Instruction** Decode, RR: Register Read, WB: Register Write Back ... Single : 24b x 24b + 73b **Integer**: 32b x 32b ... Feedback Path for Double **Precision Emulation** (65b ...
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A digital signal processor with IEEE floating-point arithmetic - group of 4 »
GRL Sohie, KL Kloker, M Inc, TX Austin - Micro, IEEE, 1988 - ieeexplore.ieee.org
... memory ports, and • an on-chip circuit **emulation** port. ... operation latencies of two to four **instruction** cycles, which ... The **precision** of the 96002's 44-bit SEP ...
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Electronic spreadsheet system and methods for compiling a formula stored in a spreadsheet into ... - group of 2 »
R Schlafly - US Patent 5,471,612, 1995 - Google Patents
... Page 8. **EXPONENT MANTISSA** |ST ST(1) ST(2) ST(3) ST(4) ST(5) ST(6) ST(7) **EXPONENT** 1MANTISSA 50 CONTROL REGISTER STATUS REGISTER **INSTRUCTION** POINTER DATA POINTER ...
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T Aamodt - 2001 - eecg.toronto.edu
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Methods for compiling formulas stored in an electronic spreadsheet system - group of 2 »
R Schlafly - US Patent 5,633,998, 1997 - Google Patents
... FIG. 3A REGISTER STRUCTURE OFINTEL-COMPATIBLE 15 **EXPONENT MANTISSA** COPROCESSORS 64 63 CONTROL REGISTER STATUS REGISTER **INSTRUCTION** POINTER DATA POINTER FIG. 3B ...
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... a second format type if a second type **instruction** consumes data produced by a first type **instruction** - group of 3 »
SG Meier, N Juffa, MD Achenbach, FD Weber... - US Patent 6,105,129, 2000 - Google Patents
... same as the corresponding significand in extended **precision**. ... PRODUCED BY A FIRST TYPE **INSTRUCTION** BACKGROUND OF ... For example, **integer** and floating point data ...
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M Coors, H Keding, O Luthje, H Meyr - EURASIP Journal on Applied Signal Processing, 2002 - hindawi.com
... a fixed word length and a fixed **exponent** to every ... information on the range and on the **precision** of the ... or **integer** word length for c. The correlation between fwl ...
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F Arakawa
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... product width is wider than the single- **precision mantissa** width, and the ... On the other hand, the **integer** multiply-add execution ... The FMAC **instruction** hardware
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... into native machine code for execution by a **floating-point unit** upon spreadsheet recalculation - group of 2 »
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A **floating point unit** for the 68040
S McCloud, D Anderson, C DeWitt, C Hinds, YW Ho, D ... - Computer Design: VLSI in Computers and Processors, 1990. ..., 1990 - ieeexplore.ieee.org
... controls data and **instruction** movement, **Integer** Unit (IU ... **instruction** normally, passing both **instruction** and data to ... is converted to extended **precision** and tagged ...
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Method and data processing system for arbitrary **precision** on numbers - group of 2 »
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... when emulating certain other arithmetic **instructions** in a ... special opera- tors for floating point math **emulation**. ... system number to maintain 30 full **precision**. ...
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Methods for compiling formulas stored in an electronic spreadsheet system - group of 2 »
R Schlafly - US Patent 5,633,998, 1997 - Google Patents
... FIG. 3A REGISTER STRUCTURE OFINTEL-COMPATIBLE 15 **EXPONENT MANTISSA** COPROCESSORS 64 63 CONTROL REGISTER STATUS REGISTER **INSTRUCTION** POINTER DATA POINTER FIG. 3B ...
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Single-**instruction**-multiple-data processing in a multimedia signal processor - group of 2 »
US Patent 6,058,465, 2000 - Google Patents
... performed to complete the **instruction**. One embodiment of the invention supports 8-bit, 9-bit, 16-bit, and 32-bit data element sizes of **integer** type for all ...
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Method and apparatus for obtaining a scalar value directly from a vector register - group of 5 »
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... a second format type if a second type **instruction** consumes data produced by a first type **instruction** - group of 3 »
SG Meier, N Juffa, MD Achenbach, FD Weber... - US Patent 6,105,129, 2000 - Google Patents
... same as the corresponding significand in extended **precision**. ... PRODUCED BY A FIRST

TYPE **INSTRUCTION** BACKGROUND OF ... For example, **integer** and floating point data ...
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... centered at E's maximum. Here, r m i r j is a tabulated 8b **integer** approximation of the distance 6 i в i m 2 ж j в j m 2 a P The peak energy: ...
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... that characterizes massively parallel computers can be SIMD (Single **Instruction** stream, Multiple ... implementation of any ANN mod- el, like the **precision** of the ...
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